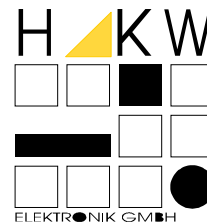


UE6011

Time-Code Receiver IC



1 Short Description

The UE6011 is a bipolar integrated straight through receiver circuit, which is suitable for the frequency range from 40kHz up to 120 kHz (ASK modulation). The receiver with built in very high sensitivity is prepared for single band reception and is designed for all kinds of radio controlled clock applications.

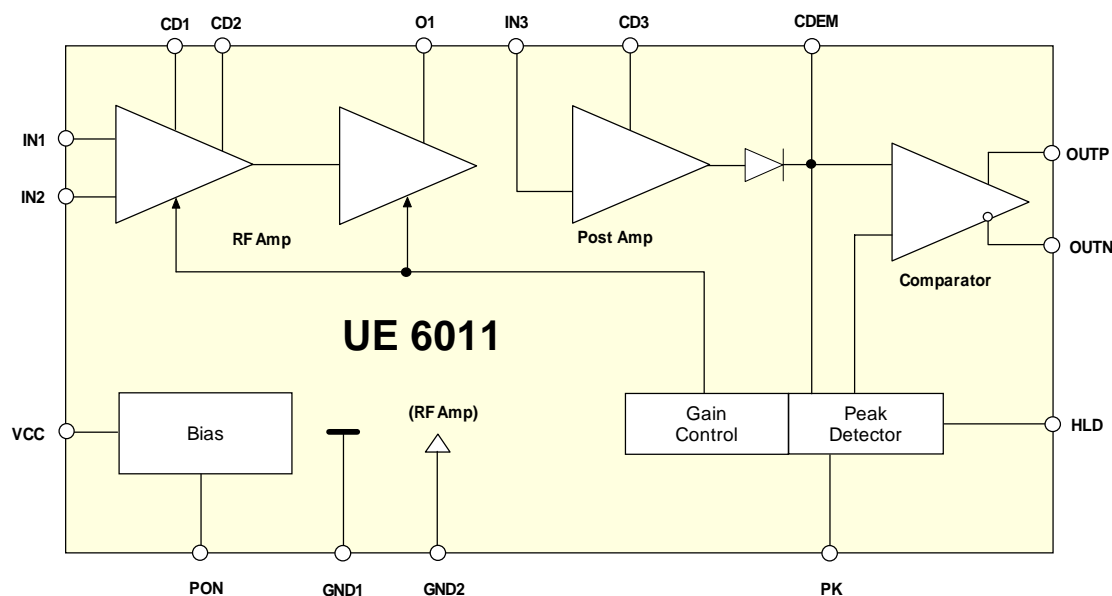
Using the corresponding peripheral circuit the IC receives and demodulates time code signals transmitted by e.g. DCF77 (Germany), MSF (UK), WWVB (USA), JJY (JPN), HBG (CH) and BPC (China).

Integrated functions as stand by mode, hold mode and complementary output stages offer features for universal applications.

2 Features

- Single Chip AM Straight Through Receiver
- Low power consumption
- Very high sensitivity (typ. $0.5\mu\text{V}$)
- High selectivity by using crystal filter
- Power down mode available
- Only a few external components necessary
- Complementary current output stages
- AGC hold mode
- Wide frequency range (40 ... 120 kHz)
- Low power battery applications (1.1 .. 3.6 V)

3 Block Diagram



4 Ordering Information

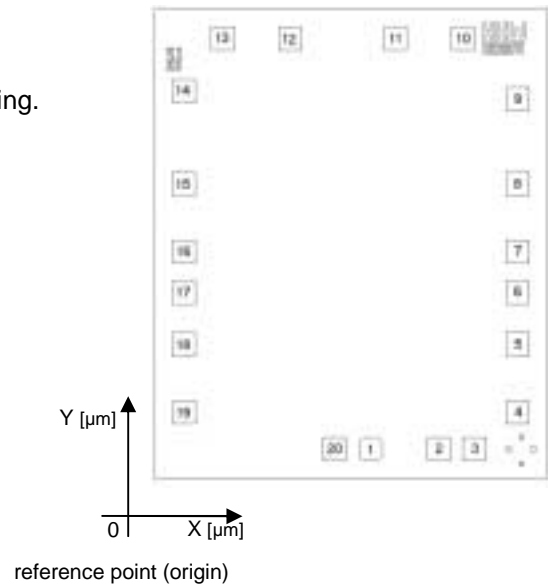
Extended Type Number	Package	Remarks
UE6011 DIT	No	Die in trace

5 Pad Layout and PAD Coordinates

The UE6011 is available as DIE for "chip-on-board" mounting.

DIE size: 1840 μm x 2210 μm
 Thickness: 460 μm
 PAD size: 110 μm x 110 μm
 min. pad-distance: 146 μm
 min. pad-pitch: 256 μm

Note:
 Pad coordinates are referred to the center point of each pad.



Symbol	Function	x-axis (μm)	y-axis (μm)	Pad # (dice)
GND2	Ground 2 (RF stages)	1104.0	219.0	1
CD1	Decoupling capacitor C1	1426.0	219.0	2
CD2	Decoupling capacitor C1	1597.0	219.0	3
IN 1	Antenna input 1	1801.0	396.0	4
IN 2	Antenna input 2	1801.0	718.0	5
VCC	Supply voltage	1801.0	964.0	6
	n.c.	1801.0	1157.0	7
OUTP	Data output (positive)	1801.0	1479.0	8
OUTN	Data output (negative)	1801.0	1881.0	9
	n.c.	1541.0	2170.0	10
GND1	Ground 1 (other stages)	1219.0	2170.0	11
HLD	AGC stop	724.0	2170.0	12
PON	Power on input	402.0	2170.0	13
PK	Peak detector output	219.0	1920.5	14
CDEM	Demodulation capacitor	219.0	1480.0	15
	n.c.	219.0	1158.0	16
	n.c.	219.0	964.0	17
CD3	Decoupling capacitor C2	219.0	718.0	18
IN3	Crystal input	219.0	396.0	19
O1	Crystal RF output	933.0	219.0	20

6 Internal connection of PAD's

The IC is ESD protected conform to the Human-Body-Model ($\pm V_{\text{ESD}} = 2000\text{V}$ on each pin referred to GND1). Ground-Pins GND1 and GND2 are internally connected to each other via the IC-substrat. We recommend to connect these pins (extern) on the PCB too.

7 Functional description of PAD's

IN 1 Antenna input 1

Both antenna inputs, IN1 and IN2, are entitled to the same rights. It is possible to realize a symmetrical operation as well as an unsymmetrical operation of the connected ferrit-antenna.

- unsymmetrical operation mode:

The HF-signal is supplied into the input IN1. The coil of the ferrit-antenna has to be connected between VCC and input IN1. Pin IN2 should be connected to VCC.

- symmetrical operation mode:

Recommended operation mode if the application is influenced by bigger disturbances. The coil of the ferrit-antenna has to be connected between IN1 and IN2. External resistors are needed to adjust the operation condition.

IN 2 Antenna input 2

The connection of IN2 is similar to that explained for IN1 .

IN 3 Crystal input

High resistance input of an amplifier stage. An external crystal has to be connected to IN3 to supply the filtered signal into this amplifier.

PON Power ON input

If PON is connected to GND, the receiver will be activated. If PON is connected to V_{CC}, the receiver will switch to power-down mode.

CD1 Decoupling capacitor C1

A capacitor is connected between CD1 and CD2. It stabilizes the operation point of the input amplifier. Expected capacitor-values: about 10...33nF.

CD2 Decoupling capacitor C1

As described for Pin CD1.

CD3 Decoupling capacitor C2

Capacitor C2 (100nF to VCC) is used to stabilize the operation point of an intermediate amplifier.

HLD AGC hold

AGC hold mode: HLD high ($V_{HLD} = V_{CC}$) sets normal function, HLD low ($V_{HLD} = 0$) holds for a short time the AGC voltage. This can be used to prevent the AGC from peak voltages, created by e.g. a stepper motor.

O1 Crystal RF output

At the output O1 you find the amplified HF-signal. O1 is connected to the crystal filter.

OUTP positive Data output

At the data output pin OUTP you find the demodulated time code signal. Output signal pulses on this pin will be HIGH-active. OUTP is a complementary current output stage. The output driving capability is about +/- 2.5µA.

OUTN negative Data output

At the data output pin OUTN you find the demodulated time code signal. Output signal pulses on this pin will be LOW-active. OUTN is a complementary current output stage. The output driving capability is about +/- 2.5µA.

PK Peak Detector output

An external capacitor has to be connected between pin PK and GND. This ensures the function of the peak detector. The value of the capacitance ($\geq 2.2\mu\text{F}$) influences the AGC regulation time.

CDEM Demodulation capacitor

Demodulator output. An external capacitor (22nF) has to be connected between pin CDEM and GND. It is used to demodulate the filtered and amplified HF-signal.

VCC Supply voltage

Positive power supply voltage of the IC.

GND1 Ground 1

GND1 is the reference potential for all IC-stages (excluding some amplifier stages) and for the internal ESD protection circuit.

GND2 Ground 2

GND2 is the reference potential for some amplifier stages (including the HF-amplifier).

8 Absolute Maximum Ratings

(for $T_{amb} = -25 \dots 85^{\circ}\text{C}$)

Pos.	Parameters	Symbol	min. value	max. value	Unit
1	Supply voltage	V_{CC}	0	5.5	V
2	allowed voltage on each pin	V_{PIN}	-0.3	$V_{CC} + 0.3$	V

9 Operation Ratings

9.1 Operation Range 1

Pos.	Parameters	Symbol	min. value	max. value	Unit
1	operation supply voltage	V_{CC}	1.1	3.6	V
2	Ambient temperature range	T_{amb}	0	50	$^{\circ}\text{C}$

9.2 Operation Range 2

Pos.	Parameters	Symbol	min. value	max. value	Unit
1	operation supply voltage	V_{CC}	1.5	3.6	V
2	Ambient temperature range	T_{amb}	-25	85	$^{\circ}\text{C}$

10 Electrical Characteristics

10.1 DC-Characteristics

test-circuitry shown in chapter 11

$V_{CC} = 3\text{V}$; $T_{amb} = 25^{\circ}\text{C}$

$V_{PON} = 0\text{V}$; $V_{STOP} = V_{CC}$

input signal V_{IN1} , $V_{IN2} = V_{CC}$; $f = 77.5\text{ kHz} \pm 5\text{ Hz}$;

AM carrier voltage reduction from 100% to 25% for $t_{MOD} = 200\text{ms}$, unless otherwise specified.

Pos.	Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
1	Quiescent current receiver OFF	$V_{PON} = V_{CC} = 3\text{V}$	I_{CC0}			1	μA
2	Supply current; receiver ON		I_{CC}	300		600	μA
3	switch current receiver ON	$V_{PON} = 0\text{V}$	$-I_{PON}$			20	μA
4	switch current; AGC in hold mode	$V_{HLD} = 0\text{V}$	$-I_{HLD}$			2	μA
5	output current (OUTx, high)	$V_{OUTx} = V_{CC} / 2$	I_{OUTx}			2.5	μA
6	output current (OUTx, low)	$V_{OUTx} = V_{CC} / 2$	$-I_{OUTx}$			2.5	μA

10.2 AC-Characteristics

test-circuitry shown in chapter 11

$V_{CC} = 3V$; $T_{amb} = 25\text{ }^{\circ}C$

$V_{PON} = 0V$; $V_{STOP} = V_{CC}$

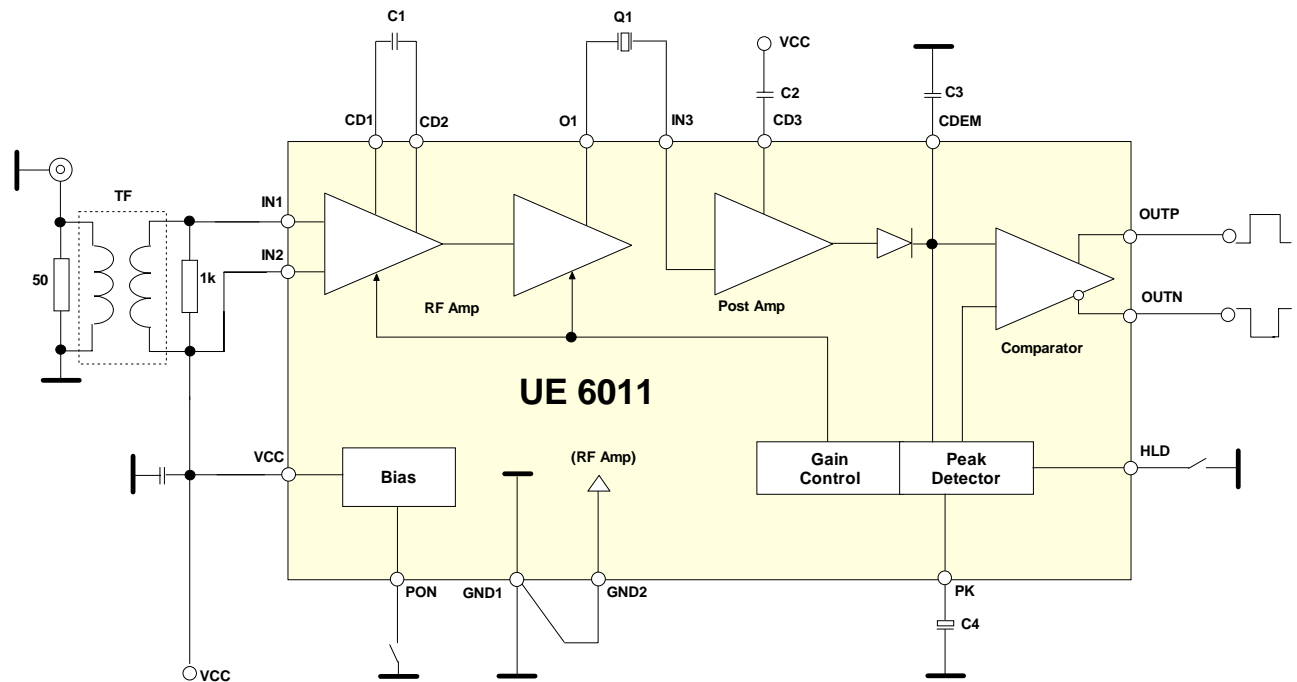
input signal V_{IN1} , $V_{IN2} = V_{CC}$; $f = 77.5\text{ kHz} \pm 5\text{ Hz}$;

AM carrier voltage reduction from 100% to 25% for $t_{MOD} = 200ms$, unless otherwise specified.

Pos.	Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
1	Minimum input voltage		$V_{IN\ min}$		0.5	0.8	μV_{RMS}
2	Maximum input voltage		$V_{IN\ max}$	30			mV_{RMS}
3	Output pulse width ¹⁾	$t_{MOD} = 100ms$	t_{WO100}	70	95	130	ms
		$t_{MOD} = 200ms$	t_{WO200}	170	195	230	ms
4	Set-up time after PON	$V_{IN} = 100\mu V$	t	3		5	s

¹⁾ specified for operation range 1

11 Test Circuitry



(TF: Schalenkern A_L 1100 nH/w^2 ; 2*25 Wdg. mit 0.2 CuL)

12 Application hints

Please refer to the separate document "UE6011-AE Vx.x" including various application hints.

13 Disclaimer of Warranty

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